

S.N. 09/955,874  
Art Unit 2819

### REMARKS

The Examiner is thanked for removing the finality of the previous rejection.

Claims 2-9, 11-13 and 15-21 are currently pending in this patent application. The latest office action states in Section 3 that claims 2, 4, 5, 6, 8, 9, 11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. 6,411,699 (Kim, newly cited). However, the body of the rejection also rejects claims 3, 7, 12 and 15-21 as being anticipated by Kim. As such, the rejection is taken to be a rejection of claims 2-9, 11-13 and 15-21 under 35 U.S.C. 102(e) as being anticipated by U.S. 6,411,699 (Kim). This rejection is respectfully disagreed with, and is traversed below.

Kim discloses digital circuitry, see Figs. 5-19, for providing a dual-modulus prescaler for an RF frequency synthesizer.

The Examiner's arguments have been carefully considered, and the claims have been amended above to highlight an important distinction between this invention and the circuitry disclosed by Kim. Note in Fig. 2 that the reference clock (VCO 36) provides a sinusoidal voltage, whereas the clock in Kim is digital (see, for example Fig. 8 of Kim). In general, this invention provides and operates analog circuitry that uses a multi-phase clock and phase rotation to generate the modulus, and eliminates the systematic error of the phase rotation system by resampling.

In order to further clarify the claims each of the independent claims has been amended above to make it clear that the output of the VCO comprises two clock signal lines, and the input to the resampler stage is also comprised of two signal lines. Reference in this regard can be made to Fig. 2. Note also page 5, line 32, to page 6, line 6:

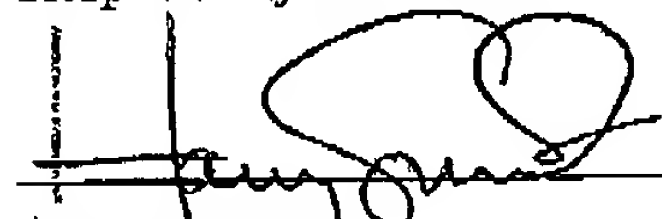
"In order to accomplish the phase comparison, the output of the VCO 36 is applied as the In\_p and In\_m signals to the inputs of the modulus prescaler 10 that was described in relation to Fig. 1."

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The amendment to the independent claims clearly and patentably distinguishes the circuitry and method in accordance with this invention from the digital circuitry embodiments disclosed by Kim, and should place all of the pending claims 2-9, 11-13 and 15-21 in condition for allowance.

The Examiner is respectfully requested to reconsider and remove the rejection based on Kim, and to allow all of the pending claims 2-9, 11-13 and 15-21.

Respectfully submitted:

  
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1/5/2004  
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